What is claimed is:

1. A mask read only memory containing diodes, comprising:

a semiconductor substrate;

an insulating layer on the semiconductor substrate;

a plurality of first conductive lines along a first direction on the insulating layer;

a plurality of vertical diodes on the first conductive lines;

a plurality of dielectric layers on part of the diodes; and

a plurality of second conductive lines along a second direction on the dielectric layers and the diodes, wherein the first direction is perpendicular to the second direction.

2. The mask read only memory containing diodes as claimed in claim 1, wherein the diodes are PN diodes.

3. The mask read only memory containing diodes as claimed in claim 2, wherein the PN diodes comprise two polysilicon layers of opposing conductive types.

4. The mask read only memory containing diodes as claimed in claim 1, wherein the insulating layer is silicon dioxide, aluminum oxide (Al_2O_3), silicon nitride (Si_3N_4), tantalum pentoxide (Ta_2O_5), barium strontium titanate (BST), hafnium oxide (HfO_2), or titanium dioxide (TiO_2).

5. The mask read only memory containing diodes as claimed in claim 1, wherein the first conductive lines are bit lines and the second conductive lines are word lines.

6. The mask read only memory containing diodes as claimed in claim 1, wherein the dielectric layers are silicon dioxide, aluminum oxide (Al_2O_3), silicon nitride (Si_3N_4), tantalum pentoxide (Ta_2O_5), barium strontium titanate (BST), hafnium oxide (HfO_2), or titanium dioxide (TiO_2).

7. The mask read only memory containing diodes as claimed in claim 1, comprising:

a semiconductor substrate;

an insulating layer on the semiconductor substrate; and

at least two memory cell layers stacked on the insulating layer wherein there is a separating layer between any two memory cell layers to provide insulation and wherein each memory cell layer comprises:

a plurality of first conductive lines along a first direction on the insulating layer;

a plurality of vertical diodes on the first conductive lines;

a plurality of dielectric layers on part of the diodes; and

a plurality of second conductive lines along a second direction on the dielectric layers

and the diodes, wherein the first direction is perpendicular to the second direction,

wherein any two adjacent upper and lower diode layers are disposed opposite to one another so that two sides thereof of opposing conductive type face each other.

8. The mask read only memory containing diodes as claimed in claim 7, which comprises 2 to 10 memory cell layers.

9. The mask read only memory containing diodes as claimed in claim 7, wherein the separating layer is silicon dioxide, aluminum oxide (Al_2O_3), silicon nitride (Si_3N_4), tantalum pentoxide (Ta_2O_5), barium strontium titanate (BST), hafnium oxide (HfO_2), or titanium dioxide (TiO_2).

10. The mask read only memory containing diodes as claimed in claim 1, comprising:

a semiconductor substrate;

an insulating layer on the semiconductor substrate;

n diode layers stacked on the insulating layer, wherein n is an integer equal to or greater than 2 and each diode layer comprises a plurality of vertical diodes and a plurality of dielectric layers on part of the diodes; and

(n + 1) parallel conductive layers disposed between the bottom diode layer and the insulating layer, on the top diode layer, and between any

two adjacent diode layers respectively, wherein the (n + 1) parallel conductive layers are disposed so that any two adjacent conductive layers are perpendicular to each other,

wherein any two adjacent upper and lower diode layers are disposed opposite to one another so that two sides of matching conductive type face each other.

11. The mask read only memory containing diodes as claimed in claim 10, wherein n is between 2 and 10.

12. A method of manufacturing mask read only memory containing diodes, comprising the steps of:

forming an insulating layer, a first conductive layer, a second conductive layer and a third conductive layer on a semiconductor substrate in order, wherein a PN junction or Schottky interface is formed between the second and the third conductive layers;

patterning the third, the second, and the first conductive layer, thereby forming a plurality of first trenches along a first direction to define the first conductive layer as a plurality of bit lines;

filling a first insulating material into the first trenches;

forming a dielectric layer on the entire surface of the third conductive layer and the first insulating material;

patterning the dielectric layer, the first insulating material, the third conductive layer and the second conductive layer and stopping the patterning at the bit lines, thereby forming a plurality of second trenches along a second direction and forming a plurality of diodes comprising the second conductive layer and the third conductive layer, wherein the first direction is perpendicular to the second direction;

filling a second insulating material into the second trenches so that the top of the second insulating material is higher than that of the dielectric layer, thereby forming a plurality of third trenches along the second direction;

patterning the dielectric layer to expose part of the third conductive layer of the diode, thereby forming a plurality of openings for coding defined as a plurality of codes; and

forming a fourth conductive layer on the entire surface of the substrate and into the third trenches and the openings for coding, thereby forming a plurality of word lines.

13. The method as claimed in claim 12, wherein the diodes are PN diodes.

14. The method as claimed in claim 13, wherein the PN diode comprises two polysilicon layers of opposing conductive types.

15. The method as claimed in claim 12, wherein the dielectric layer is silicon dioxide, aluminum oxide (Al_2O_3), silicon nitride (Si_3N_4), tantalum pentoxide (Ta_2O_5), barium strontium titanate (BST), hafnium oxide (HfO_2), or titanium dioxide (TiO_2).

16. A method of manufacturing a mask read only memory containing diodes, comprising the steps of:

forming an insulating layer, a first conductive layer, a second conductive layer, a third conductive layer, and a first dielectric layer on a semiconductor substrate in order, wherein a PN junction or Schottky interface is formed between the second and the third conductive layers;

patterning the first dielectric layer to expose part of the third conductive layer, thereby forming a plurality of first openings for coding defined as a plurality of first codes;

patterning the first dielectric layer, the third conductive layer, the second conductive layer and the first conductive layer, thereby forming a plurality of first trenches along a first direction to define the first conductive layer as a plurality of first bit lines;

filling a first insulating material into the first trenches;

forming a fourth conductive layer on the surface of the entire substrate and into the first openings for coding;

forming a fifth conductive layer, a sixth conductive layer and a second dielectric layer on the fourth conductive layer in order, wherein a PN junction or Schottky interface between the fifth and the sixth conductive layers is formed;

patterning the second dielectric layer to expose part of the sixth conductive layer, thereby forming a plurality of second openings for coding defined as a plurality of second codes;

patterning the second dielectric layer, the sixth conductive layer, the fifth conductive layer, the fourth conductive layers, the first dielectric layer, the third conductive layer, and the second conductive layer, and stopping the patterning at the first bit lines, thereby forming a plurality of second trenches along a second direction to define the fourth conductive layer as a plurality of first word lines, wherein the first direction is perpendicular to the second direction;

filling a second insulating material into the second trenches;

forming a seventh conductive layer on the surface of the entire substrate and into the second openings for coding;

forming an eighth conductive layer, a ninth conductive layer and a third dielectric layer on the seventh conductive layer in order, wherein a PN junction or Schottky interface

between the eighth and the ninth conductive layers is formed;

patterning the third dielectric layer to expose part of the ninth conductive layer, thereby forming a plurality of third openings for coding defined as a plurality of third codes;

patterning the third dielectric layer, the ninth conductive layer, the eighth conductive layer, the seventh conductive layer, the second dielectric layer, the sixth conductive layer and the fifth conductive layer, and stopping the patterning at the first word lines, thereby forming a plurality of third trenches along the first direction to define the seventh conductive layer as a plurality of second bit lines;

filling a third insulating material into the third trenches;

patterning the third dielectric layer, the ninth conductive layer and the eighth conductive layer and stopping the patterning at the second bit lines, thereby forming a plurality of fourth trenches along the second direction;

filling a fourth insulating material into the fourth trenches so that the top of the fourth insulating material is higher than that of the third dielectric layer, thereby forming a plurality of the fifth trenches along the second direction; and

filling a tenth conductive layer into the fifth trenches, thereby forming a plurality of second word lines,

wherein the third and the fifth conductive layers are of matching conductive type and the sixth and the eighth conductive layers are of matching conductive type.

17. The method as claimed in claim 16, wherein the second, the third, the fifth, the sixth, the eighth and the ninth conductive layers are doped polysilicon layers.

18. The method as claimed in claim 17, wherein the second, the sixth and the eighth conductive layers are of matching conductive type and the third, the fifth and the ninth conductive layers are of matching conductive type.

19. The method as claimed in claim 16, wherein the first, the second, and the third dielectric layers are silicon dioxide, aluminum oxide (Al_2O_3), silicon nitride (Si_3N_4), tantalum pentoxide (Ta_2O_5), barium strontium titanate (BST), hafnium oxide (HfO_2), or titanium dioxide (TiO_2).